

# SUPPOSE THE PROGRAM COUNTER (PC) IS SET TO 0x20000000.A. WHAT RANGE OF ADDRESSES CAN BE REACHED USING

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## INTRODUCTION TO THE PROGRAM COUNTER AND ADDRESSING IN MICROCONTROLLERS

THE PROGRAM COUNTER (PC) IS A FUNDAMENTAL REGISTER IN A MICROCONTROLLER OR CPU THAT KEEPS TRACK OF THE ADDRESS OF THE NEXT INSTRUCTION TO BE EXECUTED. ITS VALUE DETERMINES THE CURRENT EXECUTION POINT WITHIN THE MEMORY MAP OF THE SYSTEM. WHEN THE PC IS SET TO A SPECIFIC ADDRESS, IT INFLUENCES WHICH MEMORY LOCATIONS CAN BE ACCESSED OR EXECUTED NEXT, DIRECTLY AFFECTING PROGRAM FLOW AND DATA ACCESS.

IN EMBEDDED SYSTEMS AND MICROCONTROLLER ARCHITECTURES LIKE ARM CORTEX-M, AVR, OR PIC, UNDERSTANDING THE RANGE OF REACHABLE ADDRESSES FROM A GIVEN PC VALUE IS ESSENTIAL FOR TASKS SUCH AS DEBUGGING, MEMORY MAPPING, AND FIRMWARE DEVELOPMENT. THE STARTING ADDRESS OF 0x20000000.A (WHICH APPEARS TO BE A HEXADECIMAL VALUE WITH AN UNCONVENTIONAL FRACTIONAL COMPONENT, BUT FOR THE PURPOSE OF THIS ANALYSIS, WE INTERPRET IT AS A HEXADECIMAL ADDRESS, POSSIBLY WITH A TYPO OR FORMATTING ISSUE) INDICATES A SPECIFIC LOCATION IN MEMORY, TYPICALLY WITHIN THE SRAM OR DATA MEMORY REGION.

THIS ARTICLE EXPLORES THE IMPLICATIONS OF SETTING THE PC TO SUCH AN ADDRESS AND EXAMINES THE POTENTIAL RANGE OF MEMORY ADDRESSES THAT CAN BE REACHED FROM THAT POINT, CONSIDERING VARIOUS FACTORS SUCH AS INSTRUCTION SET ARCHITECTURE, MEMORY SIZE, ADDRESSING MODES, AND SYSTEM CONSTRAINTS.

## UNDERSTANDING THE MEMORY MAP AND ADDRESSING MODES

### MEMORY MAP OVERVIEW

MICROCONTROLLERS ORGANIZE THEIR MEMORY INTO DISTINCT REGIONS, EACH SERVING DIFFERENT PURPOSES:

- **FLASH MEMORY:** NON-VOLATILE STORAGE FOR PROGRAM CODE. TYPICALLY STARTING AT 0x00000000.
- **SRAM / DATA MEMORY:** VOLATILE MEMORY FOR RUNTIME DATA, OFTEN STARTING AT ADDRESSES LIKE 0x20000000 IN ARM CORTEX-M ARCHITECTURES.
- **PERIPHERAL REGIONS:** MEMORY-MAPPED REGISTERS FOR PERIPHERALS, SITUATED AT SPECIFIC ADDRESS RANGES.
- **EXTERNAL MEMORY:** OPTIONAL EXTERNAL MEMORY INTERFACES FOR LARGER DATA STORAGE.

GIVEN THE ADDRESS 0x20000000, IT IS MOST LIKELY WITHIN THE SRAM REGION IN ARM CORTEX-M MICROCONTROLLERS, WHICH TYPICALLY START AT 0x20000000 AND EXTEND UPWARDS DEPENDING ON THE DEVICE.

# ADDRESSING MODES AND INSTRUCTION SET CONSTRAINTS

THE SET OF ADDRESSES THAT CAN BE REACHED FROM A GIVEN PC DEPENDS ON THE INSTRUCTION SET AND ADDRESSING MODES SUPPORTED:

- **PC-RELATIVE ADDRESSING:** BRANCH INSTRUCTIONS THAT SPECIFY AN OFFSET FROM THE CURRENT PC.
- **ABSOLUTE ADDRESSING:** JUMP OR CALL INSTRUCTIONS THAT SPECIFY AN EXPLICIT MEMORY ADDRESS.
- **INDIRECT ADDRESSING:** USING REGISTERS OR MEMORY POINTERS TO ACCESS DATA OR CODE.

THE ARCHITECTURE'S INSTRUCTION SET DETERMINES HOW FAR AND IN WHAT MANNER THE PC CAN JUMP OR BRANCH TO OTHER ADDRESSES.

## ANALYZING THE REACHABLE ADDRESS RANGE FROM 0x20000000.A

### INTERPRETING THE STARTING ADDRESS

THE ADDRESS 0x20000000.A APPEARS TO BE A HEXADECIMAL VALUE WITH A FRACTIONAL COMPONENT, WHICH IS UNUSUAL IN MEMORY ADDRESSING. SINCE ADDRESSES ARE INTEGRAL, WE INTERPRET THIS AS 0x20000000 OR POSSIBLY 0x20000000 WITH AN OFFSET, OR PERHAPS A TYPO.

ASSUMING THE STARTING ADDRESS IS 0x20000000, THE FOLLOWING CONSIDERATIONS APPLY:

- THE INITIAL ADDRESS IS WITHIN THE SRAM REGION OF THE MICROCONTROLLER.
- THE RANGE OF ADDRESSES REACHABLE DEPENDS ON THE INSTRUCTION EXECUTION FLOW, BRANCH OFFSETS, AND THE SIZE OF THE PROGRAM.

### POTENTIAL RANGE OF REACHABLE ADDRESSES

THE REACHABLE ADDRESSES DEPEND ON THE MAXIMUM OFFSET ALLOWED IN BRANCH INSTRUCTIONS, THE SIZE OF THE PROGRAM, AND THE SYSTEM'S MEMORY MAP.

#### BRANCH AND JUMP INSTRUCTION LIMITS

IN ARM CORTEX-M ARCHITECTURES, FOR EXAMPLE:

- **BRANCH INSTRUCTIONS** OFTEN SUPPORT SIGNED 12-BIT OR 24-BIT OFFSETS.
- **ABSOLUTE JUMPS** CAN SPECIFY ANY ADDRESS WITHIN THE ADDRESSABLE RANGE, SUBJECT TO THE ARCHITECTURE'S LIMITATIONS.

GIVEN A BRANCH WITH A 12-BIT SIGNED OFFSET, THE MAXIMUM FORWARD OR BACKWARD JUMP IS APPROXIMATELY  $\pm 4\text{KB}$  (4096 BYTES). FOR LARGER JUMPS, INDIRECT OR ABSOLUTE ADDRESSING MODES ARE USED.

#### MEMORY RANGE BASED ON INSTRUCTION CONSTRAINTS

ASSUMING THE PROGRAM IS EXECUTING FROM 0x20000000 AND USING BRANCH INSTRUCTIONS WITH  $\pm 4\text{KB}$ :

- MINIMUM REACHABLE ADDRESS:  $0x20000000 - 0x1000 = 0x1FFFF000$  (IF BACKWARD BRANCH IS PERMITTED).
- MAXIMUM REACHABLE ADDRESS:  $0x20000000 + 0x1000 = 0x20001000$  (IF FORWARD BRANCH IS USED).

HOWEVER, IF ABSOLUTE JUMPS OR FUNCTION CALLS ARE USED, THEN THE PROGRAM CAN POTENTIALLY REACH ANY ADDRESS WITHIN THE SRAM OR CODE REGION, LIMITED BY THE TOTAL SIZE OF AVAILABLE MEMORY.

## MEMORY REGION CONSTRAINTS

- SRAM SIZE: COMMON MICROCONTROLLERS MAY HAVE SRAM REGIONS STARTING AT  $0x20000000$  WITH SIZES RANGING FROM A FEW KILOBYTES TO SEVERAL MEGABYTES.
- PROGRAM SIZE: THE SIZE OF THE FIRMWARE DETERMINES HOW MUCH MEMORY IS OCCUPIED AND WHAT ADDRESSES ARE ACCESSIBLE.
- PERIPHERAL AND EXTERNAL MEMORY BOUNDARIES: THESE ARE TYPICALLY OUTSIDE THE SRAM REGION AND REQUIRE SPECIFIC INSTRUCTIONS OR HARDWARE SUPPORT TO ACCESS.

## PRACTICAL IMPLICATIONS AND EXAMPLES

### EXAMPLE 1: ARM CORTEx-M MICROCONTROLLER

SUPPOSE THE MICROCONTROLLER HAS:

- SRAM STARTING AT  $0x20000000$
- SRAM SIZE: 128 KB ( $0x20000$  BYTES)
- THE PROGRAM IS EXECUTING AT  $0x20000000$

FROM THIS SETUP:

- THE ADDRESS RANGE OF SRAM IS  $0x20000000$  TO  $0x20020000$
- THE PROGRAM CAN, WITH THE RIGHT INSTRUCTIONS, REACH ANY ADDRESS WITHIN THIS RANGE

BRANCH INSTRUCTIONS WITH LIMITED OFFSET SUPPORT RESTRICT HOW FAR THE PROGRAM CAN JUMP DIRECTLY. FOR LARGER JUMPS, INDIRECT ADDRESSING OR FUNCTION CALLS ARE USED.

### EXAMPLE 2: JUMPING TO EXTERNAL ADDRESSES

IF THE PROGRAM SUPPORTS EXTERNAL MEMORY ACCESS OR HAS A JUMP TABLE, IT COULD REACH ADDRESSES OUTSIDE THE SRAM, PROVIDED THE HARDWARE AND INSTRUCTION SET SUPPORT SUCH OPERATIONS.

## FACTORS AFFECTING REACHABILITY

VARIOUS FACTORS INFLUENCE WHICH ADDRESSES CAN BE REACHED FROM A GIVEN PC VALUE:

1. **INSTRUCTION SET ARCHITECTURE (ISA):** DETERMINES THE MAXIMUM OFFSET AND ADDRESSING MODES SUPPORTED.

2. **MEMORY MAP AND SIZE:** THE TOTAL SIZE AND LAYOUT OF MEMORY REGIONS DEFINE BOUNDARIES.
3. **PROGRAM SIZE AND STRUCTURE:** THE AVAILABLE CODE AND DATA INFLUENCE ACCESSIBLE ADDRESSES.
4. **COMPILER AND ASSEMBLER CONSTRAINTS:** HOW CODE IS GENERATED IMPACTS JUMP RANGES.
5. **HARDWARE LIMITATIONS:** EXTERNAL MEMORY INTERFACES, MEMORY PROTECTION UNITS, AND OTHER HARDWARE FEATURES CAN RESTRICT OR ENABLE ACCESS TO CERTAIN ADDRESSES.

## SUMMARY AND CONCLUSION

STARTING FROM AN ADDRESS LIKE `0x20000000`, THE RANGE OF ADDRESSES THAT CAN BE REACHED DEPENDS PRIMARILY ON THE ARCHITECTURE'S INSTRUCTION SET, MEMORY MAP, AND PROGRAM FLOW CONTROL MECHANISMS. IN MOST EMBEDDED SYSTEMS, ESPECIALLY ARM CORTEX-M MICROCONTROLLERS, THE SRAM REGION STARTING AT `0x20000000` TYPICALLY SPANS A KNOWN SIZE, SUCH AS 64 KB, 128 KB, OR MORE.

BRANCH INSTRUCTIONS WITHIN THE CPU'S INSTRUCTION SET SUPPORT LIMITED OFFSETS, OFTEN IN THE ORDER OF A FEW KILOBYTES, WHICH CONSTRAINS DIRECT JUMPS. FOR BROADER ADDRESS TRANSITIONS—SUCH AS JUMPING TO CODE IN FLASH MEMORY, EXTERNAL MEMORY, OR OTHER PERIPHERALS—SPECIAL INSTRUCTIONS, INDIRECT ADDRESSING, OR FULL ABSOLUTE JUMPS ARE USED.

IN CONCLUSION, FROM A STARTING PC OF `0x20000000`, THE PROGRAM CAN DIRECTLY REACH ADDRESSES WITHIN THE SAME MEMORY REGION, CONSTRAINED BY INSTRUCTION-SPECIFIC OFFSETS AND THE TOTAL SIZE OF THE SRAM. INDIRECT JUMPS OR FUNCTION CALLS CAN EXTEND REACHABILITY TO ANY ADDRESS WITHIN THE ACCESSIBLE MEMORY MAP, ALLOWING FLEXIBLE PROGRAM FLOW. UNDERSTANDING THESE LIMITATIONS AND CAPABILITIES IS CRUCIAL FOR EMBEDDED SYSTEM DESIGN, DEBUGGING, AND FIRMWARE DEVELOPMENT.

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NOTE: TO PRECISELY DETERMINE THE REACHABLE ADDRESS RANGE IN A SPECIFIC SYSTEM, CONSULT THE DEVICE'S DATASHEET, REFERENCE MANUAL, AND THE COMPILER'S ARCHITECTURE-SPECIFIC DOCUMENTATION, AS THESE PROVIDE EXACT DETAILS ON ADDRESSING MODES, MEMORY SIZES, AND INSTRUCTION SET LIMITATIONS.

## FREQUENTLY ASKED QUESTIONS

### WHAT IS THE SIGNIFICANCE OF SETTING THE PROGRAM COUNTER (PC) TO `0x20000000` IN A SYSTEM?

SETTING THE PC TO `0x20000000` INITIALIZES THE PROCESSOR TO START EXECUTING INSTRUCTIONS FROM THAT SPECIFIC MEMORY ADDRESS, WHICH IS TYPICALLY WITHIN A CERTAIN MEMORY REGION LIKE RAM OR A SPECIFIC MEMORY MAP IN EMBEDDED SYSTEMS.

### HOW DO YOU DETERMINE THE RANGE OF ADDRESSES REACHABLE FROM THE PC SET TO `0x20000000`?

THE REACHABLE ADDRESS RANGE DEPENDS ON THE INSTRUCTION SET ARCHITECTURE, MEMORY SIZE, AND ANY ADDRESSING MODES OR LIMITATIONS. USUALLY, IT INCLUDES ADDRESSES WITHIN THE BOUNDS OF THE MEMORY MAPPED TO THE PROGRAM'S EXECUTION AREA.

## IF THE PROGRAM USES 32-BIT ADDRESSING, WHAT IS THE MAXIMUM ADDRESS RANGE ACCESSIBLE FROM 0x20000000?

WITH 32-BIT ADDRESSING, THE MAXIMUM ADDRESS SPACE IS FROM 0x00000000 TO 0xFFFFFFFF. THE REACHABLE RANGE FROM 0x20000000 DEPENDS ON THE PROGRAM'S CODE AND DATA SIZE, BUT THEORETICALLY SPANS FROM 0x20000000 UP TO THE MAXIMUM ADDRESS, SUBJECT TO MEMORY CAPACITY.

## WHAT FACTORS LIMIT THE RANGE OF ADDRESSES ACCESSIBLE FROM A SPECIFIC PC VALUE LIKE 0x20000000?

FACTORS INCLUDE THE SIZE OF AVAILABLE MEMORY, THE PROCESSOR'S ADDRESSING CAPABILITIES, MEMORY MAPPING, AND ANY HARDWARE OR SOFTWARE RESTRICTIONS SUCH AS MEMORY PROTECTION OR SEGMENTATION.

## IN EMBEDDED SYSTEMS, WHAT IS TYPICALLY THE ADDRESS RANGE STARTING AT 0x20000000?

IN MANY EMBEDDED SYSTEMS, ADDRESSES STARTING AT 0x20000000 OFTEN CORRESPOND TO SRAM OR RAM REGIONS, MEANING THE PROGRAM CAN ACCESS ADDRESSES WITHIN THIS RANGE FOR DATA STORAGE AND EXECUTION, LIMITED BY THE SIZE OF THE RAM CHIP.

## HOW DOES THE INSTRUCTION SET ARCHITECTURE INFLUENCE THE REACHABLE ADDRESS RANGE FROM A GIVEN PC VALUE?

THE ISA DETERMINES HOW INSTRUCTIONS ARE FORMATTED, INCLUDING THEIR ADDRESSING MODES, WHICH IN TURN DEFINES HOW FAR AND IN WHAT WAYS THE PROGRAM CAN ACCESS MEMORY ADDRESSES RELATIVE TO THE PC. SOME ARCHITECTURES SUPPORT ONLY RELATIVE ADDRESSING, LIMITING REACH, WHILE OTHERS SUPPORT ABSOLUTE ADDRESSING ACROSS THE ENTIRE ADDRESS SPACE.

## CAN THE RANGE OF ADDRESSES REACHABLE FROM 0x20000000 BE EXTENDED, AND IF SO, HOW?

YES, THE REACHABLE ADDRESS RANGE CAN BE EXTENDED BY INCREASING THE AVAILABLE MEMORY, CHANGING MEMORY MAPPING CONFIGURATIONS, OR MODIFYING THE PROGRAM TO UTILIZE DIFFERENT ADDRESSING MODES OR MEMORY SEGMENTS SUPPORTED BY THE HARDWARE AND ARCHITECTURE.

## ADDITIONAL RESOURCES

SUPPOSE THE PROGRAM COUNTER (PC) IS SET TO 0x20000000. WHAT RANGE OF ADDRESSES CAN BE REACHED USING

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### INTRODUCTION

IN THE REALM OF COMPUTER ARCHITECTURE AND EMBEDDED SYSTEMS, UNDERSTANDING HOW THE PROGRAM COUNTER (PC) INFLUENCES THE ADDRESS SPACE ACCESSIBLE BY A PROCESSOR IS FUNDAMENTAL. THE PC, OFTEN REFERRED TO AS THE INSTRUCTION POINTER, DETERMINES THE NEXT INSTRUCTION TO EXECUTE BY HOLDING A MEMORY ADDRESS. WHEN THE PC IS INITIALIZED OR SET TO A SPECIFIC VALUE, SUCH AS 0x20000000, THE IMMEDIATE QUESTION ARISES: WHAT RANGE OF ADDRESSES CAN THE PROCESSOR REACH FROM THIS STARTING POINT?

THIS INQUIRY IS NOT MERELY ACADEMIC; IT FORMS THE BACKBONE OF SYSTEM DESIGN, MEMORY MANAGEMENT, AND SECURITY ANALYSIS IN EMBEDDED DEVICES, MICROCONTROLLERS, AND MORE COMPLEX COMPUTING SYSTEMS. THIS ARTICLE DELVES INTO THE MECHANICS OF ADDRESS CALCULATION BASED ON THE PC'S POSITION, CONSIDERING SYSTEM ARCHITECTURE, MEMORY MAPPING, AND CONSTRAINTS IMPOSED BY HARDWARE AND SOFTWARE.

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## UNDERSTANDING ADDRESSING AND THE PROGRAM COUNTER

BEFORE EXPLORING SPECIFIC ADDRESS RANGES, IT IS ESSENTIAL TO UNDERSTAND THE FUNDAMENTAL ROLE OF THE PC WITHIN A COMPUTING SYSTEM.

### THE ROLE OF THE PROGRAM COUNTER

- DEFINITION: THE PROGRAM COUNTER (PC) IS A REGISTER WITHIN A CPU THAT HOLDS THE MEMORY ADDRESS OF THE NEXT INSTRUCTION TO EXECUTE.
- FUNCTIONALITY: DURING INSTRUCTION FETCH CYCLES, THE CPU READS THE INSTRUCTION FROM THE ADDRESS IN THE PC. POST-FETCH, IT UPDATES THE PC BASED ON CONTROL FLOW, SUCH AS INCREMENTING SEQUENTIALLY OR JUMPING TO A DIFFERENT ADDRESS, DEPENDING ON THE INSTRUCTION.

### ARCHITECTURE TYPES AND ADDRESS BUS WIDTH

- ADDRESS BUS WIDTH: THE SIZE OF THE ADDRESS BUS DETERMINES THE MAXIMUM ADDRESSABLE MEMORY SPACE.
- FOR EXAMPLE, A 32-BIT ADDRESS BUS CAN ADDRESS UP TO  $2^{32}$  BYTES (4 GB).
- A 24-BIT ADDRESS BUS CAN ADDRESS UP TO  $2^{24}$  BYTES (16 MB).
- IMPACT ON REACHABILITY: THE RANGE OF ADDRESSES REACHABLE FROM A GIVEN PC VALUE DEPENDS HEAVILY ON THE ARCHITECTURE'S ADDRESS BUS WIDTH AND THE ADDRESSING MODE.

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### THE SIGNIFICANCE OF THE STARTING ADDRESS: 0x20000000

THE SPECIFIC VALUE 0x20000000 IS A HEXADECIMAL NOTATION REPRESENTING A PARTICULAR MEMORY ADDRESS. ITS SIGNIFICANCE CAN VARY BASED ON ARCHITECTURE, BUT IN MANY EMBEDDED SYSTEMS, ESPECIALLY THOSE INVOLVING ARM CORTEX-M MICROCONTROLLERS, ADDRESSES STARTING WITH 0x2000.... ARE TYPICALLY MAPPED TO SRAM OR INTERNAL RAM REGIONS.

### CONTEXTUAL EXAMPLES OF 0x20000000

- ARM CORTEX-M MICROCONTROLLERS: THE 0x20000000 BASE ADDRESS OFTEN SIGNIFIES THE BEGINNING OF SRAM.
- MEMORY MAP VARIABILITY: DIFFERENT MICROCONTROLLERS AND PROCESSORS HAVE UNIQUE MEMORY MAPS, BUT THE STARTING ADDRESS USUALLY INDICATES A SPECIFIC MEMORY REGION.

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### ADDRESS RANGE DETERMINATION: FACTORS AND CONSTRAINTS

TO UNDERSTAND WHAT ADDRESSES CAN BE REACHED FROM 0x20000000, SEVERAL FACTORS MUST BE CONSIDERED:

#### 1. ADDRESS BUS WIDTH AND MEMORY MAP

- THE MAXIMUM ADDRESSABLE MEMORY DEPENDS ON THE ARCHITECTURE'S ADDRESS BUS.
- FOR EXAMPLE:
- 32-BIT ARCHITECTURE: CAN THEORETICALLY ACCESS ADDRESSES FROM 0x00000000 UP TO 0xFFFFFFFF (4 GB).
- 16-BIT ARCHITECTURE: LIMITS ADDRESSES FROM 0x0000 TO 0xFFFF (64 KB).

IMPLICATION: IF THE ARCHITECTURE SUPPORTS 32-BIT ADDRESSES, STARTING FROM 0x20000000, THE PROCESSOR CAN THEORETICALLY REACH ANY ADDRESS WITHIN 0x20000000 TO 0xFFFFFFFF, UNLESS RESTRICTED BY HARDWARE OR SOFTWARE.

#### 2. MEMORY MAP AND HARDWARE LIMITATIONS

- PHYSICAL MEMORY: NOT ALL ADDRESS SPACE IS NECESSARILY MAPPED TO PHYSICAL MEMORY; SOME REGIONS ARE RESERVED

FOR PERIPHERALS OR ARE UNMAPPED.

- MEMORY PROTECTION: CERTAIN ADDRESSES MAY BE PROTECTED OR INACCESSIBLE DEPENDING ON PRIVILEGE LEVELS OR SECURITY FEATURES.

### 3. ADDRESSING MODES AND INSTRUCTION SET

- RELATIVE ADDRESSING: MANY INSTRUCTIONS USE RELATIVE OFFSETS, MEANING THE REACHABLE ADDRESS RANGE DEPENDS ON THE SIZE OF THE OFFSET FIELD.
- ABSOLUTE ADDRESSING: ALLOWS JUMPING OR ACCESSING ANY ADDRESS WITHIN THE ADDRESS BUS WIDTH.

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#### PRACTICAL REACHABLE ADDRESS RANGE: A DEEP DIVE

GIVEN THE STARTING POINT OF 0x20000000, WHAT IS THE THEORETICAL AND PRACTICAL RANGE OF ADDRESSES ACCESSIBLE?

##### THEORETICAL RANGE

- MAXIMUM ADDRESSABILITY: IN A 32-BIT ARCHITECTURE, ADDRESSES RANGE FROM 0x00000000 TO 0xFFFFFFFF.
- FROM 0x20000000: THE PROCESSOR CAN REACH ANY ADDRESS WITHIN THIS RANGE, SUBJECT TO HARDWARE CONSTRAINTS.

##### CALCULATIONS:

- TOTAL ADDRESS SPACE: 4,294,967,296 BYTES (4 GB).
- STARTING POINT: 0x20000000 (WHICH IS 536,870,912 IN DECIMAL).

##### POTENTIAL REACH:

- UP TO 0xFFFFFFFF (4,294,967,295):
- ADDRESS RANGE: 0x20000000 TO 0xFFFFFFFF.
- THE SIZE OF THIS RANGE:

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$0xFFFFFFFF - 0x20000000 + 1 = (4294967295 - 536870912 + 1) = 3758096384$  BYTES (~3.5 GB)

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##### SUMMARY:

FROM 0x20000000, THE PROCESSOR CAN POTENTIALLY REACH ADDRESSES UP TO 0xFFFFFFFF, COVERING APPROXIMATELY 3.5 GB OF ADDRESS SPACE.

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#### PRACTICAL LIMITATIONS AND CONSIDERATIONS

WHILE THE THEORETICAL MAXIMUM IS EXTENSIVE, PRACTICAL LIMITATIONS OFTEN REDUCE THE REACHABLE ADDRESS RANGE:

##### 1. MEMORY MAP RESTRICTIONS

- MANY EMBEDDED SYSTEMS HAVE DEDICATED REGIONS FOR RAM, FLASH, PERIPHERALS, AND OTHER DEVICES.
- FOR EXAMPLE, IN ARM CORTEX-M MICROCONTROLLERS, THE 0x20000000 REGION TYPICALLY MAPS TO SRAM, WITH THE SIZE SPECIFIED IN DATASHEETS (E.G., 64 KB, 128 KB).

##### EXAMPLE:

IF THE SRAM IS 128 KB STARTING AT 0x20000000, THEN:

- ADDRESS RANGE: 0x20000000 TO 0x2001FFFF.

## 2. MEMORY PROTECTION UNITS (MPUs)

- ENFORCED BY HARDWARE, MPUs CAN RESTRICT ACCESS TO CERTAIN REGIONS.
- EVEN IF THE ARCHITECTURE ALLOWS REACHING HIGH ADDRESSES, ACCESS MAY BE BLOCKED.

## 3. SOFTWARE CONSTRAINTS

- THE OPERATING SYSTEM OR FIRMWARE MAY LIMIT ACCESSIBLE REGIONS TO PREVENT CORRUPTION OR UNAUTHORIZED ACCESS.
- JUMP INSTRUCTIONS OR POINTER ARITHMETIC ARE OFTEN CONSTRAINED BY INSTRUCTION LENGTH AND MODE.

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## ADDRESS REACHABILITY IN DIFFERENT ARCHITECTURES

IT'S CRUCIAL TO RECOGNIZE THAT THE IMPLICATIONS OF SETTING THE PC TO 0x20000000 VARY ACROSS ARCHITECTURES.

### ARM CORTEx-M MICROCONTROLLERS

- MEMORY MAP:
  - 0x20000000 TO 0x2003FFFF: SRAM (UP TO 256 KB)
  - 0x08000000 TO 0x087FFFFF: FLASH MEMORY
  - 0x40000000 AND ABOVE: PERIPHERALS
- REACHABILITY:
  - LIMITED TO MAPPED REGIONS; THE PC CAN ONLY REACH ADDRESSES MAPPED TO EXECUTABLE MEMORY.

### 16-BIT MICROCONTROLLERS (E.G., PIC, 8051)

- ADDRESS SPACE:
  - LIMITED TO 16-BIT ADDRESSES (0x0000 TO 0xFFFF).
- IMPLICATION:
  - STARTING AT 0x20000000 IS NOT APPLICABLE; ADDRESSES WRAP AROUND OR ARE CONSTRAINED.

### 32-BIT SYSTEMS (E.G., x86, ARM CORTEx-A)

- ADDRESSING:
  - CAN REACH THE ENTIRE 4 GB ADDRESS SPACE, SUBJECT TO HARDWARE AND OS RESTRICTIONS.

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## JUMPING AND BRANCHING CAPABILITIES FROM 0x20000000

UNDERSTANDING REACHABILITY ALSO INVOLVES EXAMINING INSTRUCTION CAPABILITIES:

- BRANCH INSTRUCTIONS: OFTEN LIMITED TO A CERTAIN OFFSET RANGE (E.G.,  $\pm 2$  KB,  $\pm 4$  MB) DEPENDING ON INSTRUCTION ENCODING.
- ABSOLUTE JUMPS: CAN TARGET ANY ADDRESS WITHIN THE ADDRESS BUS WIDTH.

EXAMPLE:

IN ARM THUMB MODE, RELATIVE BRANCH OFFSETS ARE LIMITED, BUT ABSOLUTE JUMPS VIA BRANCH AND LINK INSTRUCTIONS CAN TARGET ANY ADDRESS IN THE MAPPED EXECUTABLE REGIONS.

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## SECURITY AND SAFETY IMPLICATIONS

KNOWING THE ADDRESS RANGE ACCESSIBLE FROM A PARTICULAR PC VALUE IS CRITICAL FOR:

- SECURITY: PREVENTING UNAUTHORIZED CODE EXECUTION OUTSIDE PERMITTED REGIONS.

- SYSTEM STABILITY: AVOIDING JUMPS INTO UNMAPPED OR RESERVED MEMORY, WHICH CAN CAUSE FAULTS.
- DEBUGGING: TRACING ADDRESS REACHABILITY TO DIAGNOSE FAULTS OR BUGS.

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## SUMMARY AND CONCLUSIONS

SUPPOSE THE PROGRAM COUNTER (PC) IS SET TO 0x20000000. WHAT RANGE OF ADDRESSES CAN BE REACHED USING?

- THEORETICALLY, IN A 32-BIT ARCHITECTURE WITH FULL ADDRESS BUS SUPPORT, THE PC CAN REACH FROM 0x20000000 UP TO 0xFFFFFFFF, COVERING ROUGHLY 3.5 GB OF ADDRESS SPACE.
- PRACTICALLY, THE REACHABLE ADDRESSES ARE LIMITED BY:
  - THE SYSTEM'S MEMORY MAP (E.G., SRAM, FLASH, PERIPHERAL REGIONS).
  - HARDWARE CONSTRAINTS SUCH AS ADDRESS DECODING AND MEMORY PROTECTION UNITS.
  - SOFTWARE RESTRICTIONS IMPOSED BY THE OPERATING SYSTEM OR FIRMWARE.
  - INSTRUCTION SET LIMITATIONS ON RELATIVE AND ABSOLUTE ADDRESSING MODES.
- IN SPECIFIC SYSTEMS LIKE ARM CORTEX-M MICROCONTROLLERS, STARTING AT 0x20000000 OFTEN INDICATES SRAM, WHICH MAY BE LIMITED IN SIZE (E.G., 64 KB OR 128 KB), THUS RESTRICTING THE REACHABLE ADDRESSES TO THAT REGION.
- IN MORE GENERAL TERMS, THE STARTING ADDRESS PROVIDES A BASELINE, BUT THE EFFECTIVE RANGE DEPENDS ON THE ARCHITECTURE, MEMORY MAP, AND OPERATIONAL CONTEXT.

UNDERSTANDING THESE NUANCES IS VITAL FOR SYSTEM DESIGNERS, EMBEDDED DEVELOPERS, AND SECURITY PROFESSIONALS AIMING TO OPTIMIZE, SECURE, AND TROUBLESHOOT

## **Suppose The Program Counter Pc Is Set To 0x20000000 A What Range Of Addresses Can Be Reached Using**

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